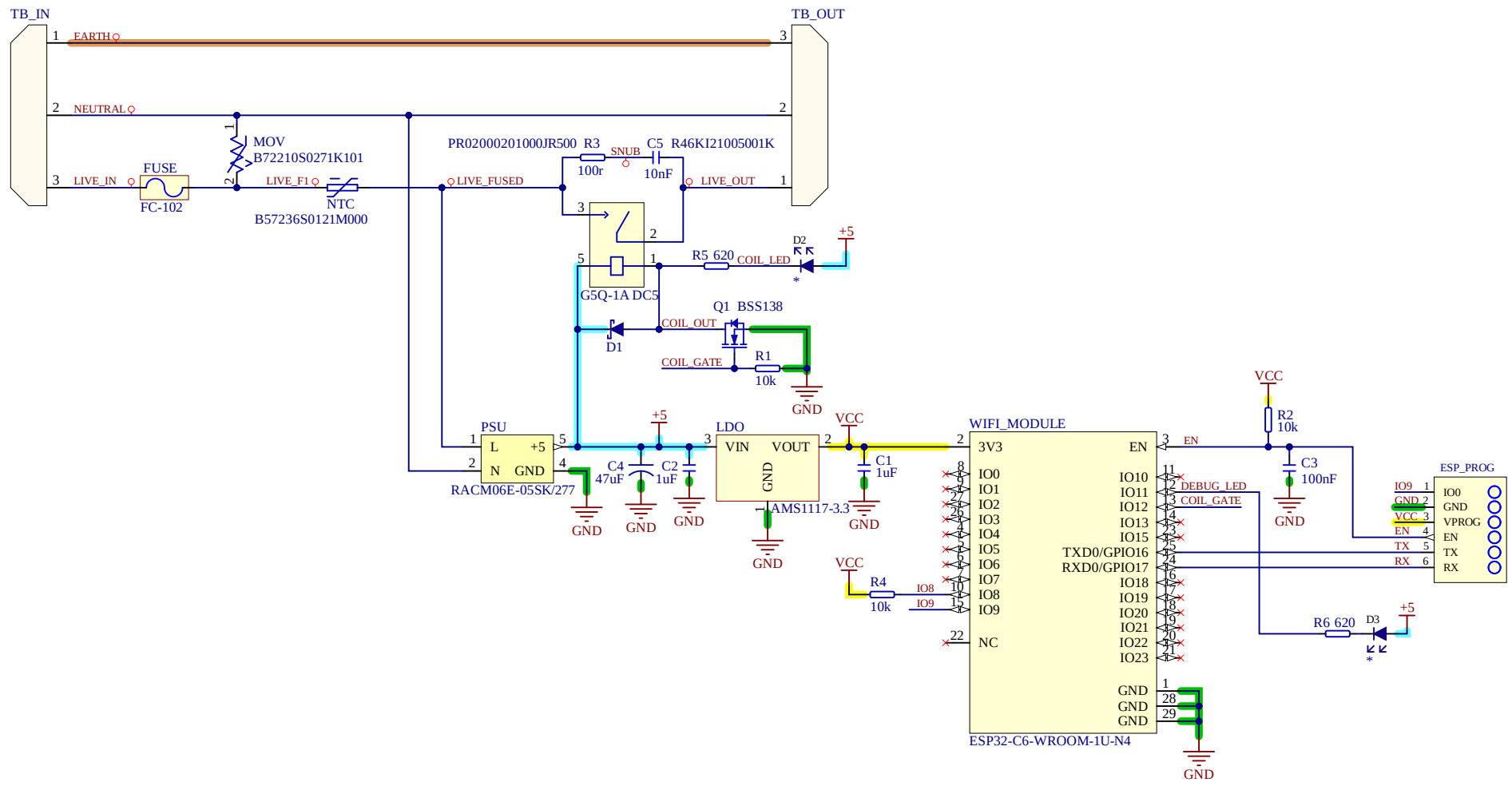




WifiSwitch

[chs](#)

Saved on 18 May 2026

Sheet 1 of 1

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for

Design Rules Verification Report

Filename : E:\dev\WifiSwitch\PCB\WifiSwitch.PcbDoc

Warnings 0
Rule Violations 6

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=2.5mm) (InNetClass('MAINS')), (Not InNet('GND'))	0
Clearance Constraint (Gap=0.102mm) (All), (All)	0
Short-Circuit Constraint (Allowed=No) (All), (All)	0
Un-Routed Net Constraint (All)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.127mm) (Max=3mm) (Preferred=0.254mm) (All	0
Routing Topology Rule(Topology=Shortest) (All)	0
Routing Via (Templates Used To Check Via: GND_STITCH, THERMAL) (All	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	6
Hole To Hole Clearance (Gap=0.254mm) (All), (All)	0
Minimum Solder Mask Sliver (Gap=0.127mm) (All), (All)	0
Silk To Solder Mask (Clearance=0mm) (IsPad), (All)	0
Silk to Silk (Clearance=0mm) (All), (All)	0
Net Antennae (Tolerance=0mm) (All)	0
Component Clearance Constraint (Horizontal Gap = 0mm, Vertical Gap = 0mm) (All), (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All	0
Total	6

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	
Hole Size Constraint: (3mm > 2.54mm) Pad Free-M(3mm,3mm) on Multi-Layer Actual Hole Size = 3mm	
Hole Size Constraint: (3mm > 2.54mm) Pad Free-M(3mm,59mm) on Multi-Layer Actual Hole Size = 3mm	
Hole Size Constraint: (3mm > 2.54mm) Pad Free-M(49.75mm,3mm) on Multi-Layer Actual Hole Size = 3mm	
Hole Size Constraint: (3mm > 2.54mm) Pad Free-M(49.75mm,59mm) on Multi-Layer Actual Hole Size = 3mm	
Hole Size Constraint: (3mm > 2.54mm) Pad Free-M(96.5mm,3mm) on Multi-Layer Actual Hole Size = 3mm	
Hole Size Constraint: (3mm > 2.54mm) Pad Free-M(96.5mm,59mm) on Multi-Layer Actual Hole Size = 3mm	

