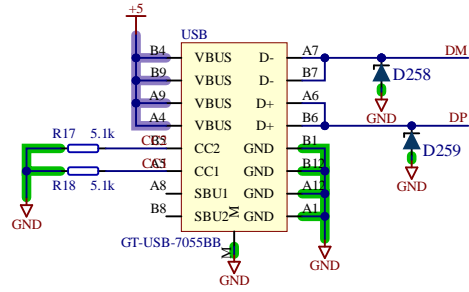
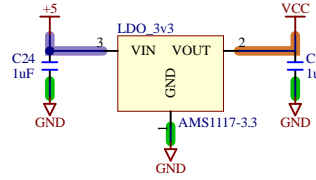


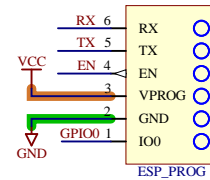
USB Connector



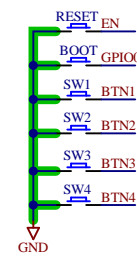
3.3V LDO



ESP Prog header



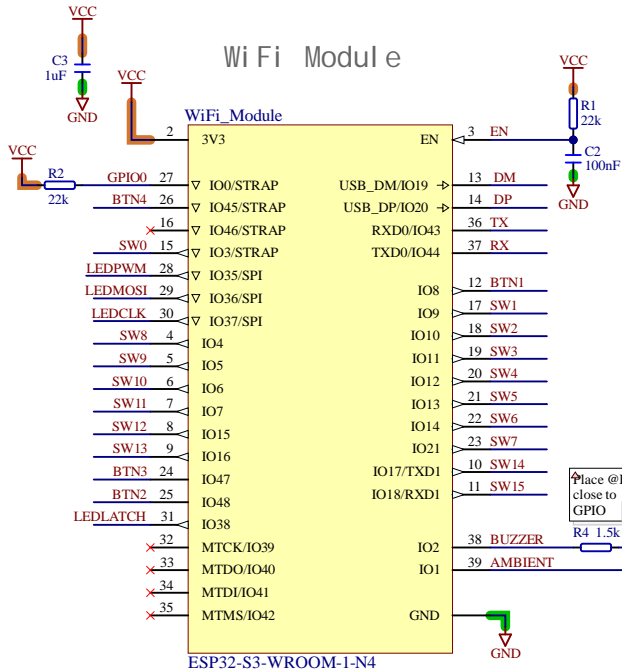
Buttons



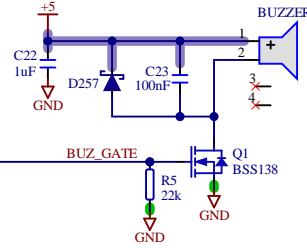
Cathode debounce



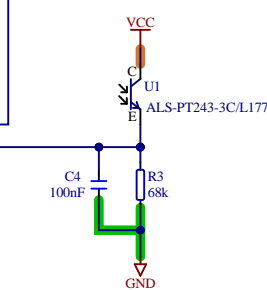
Wi Fi Module



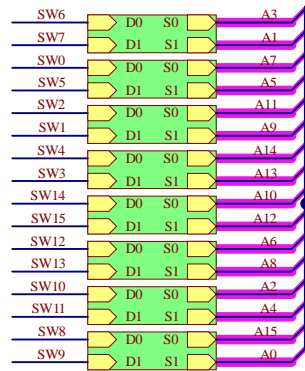
Buzzer



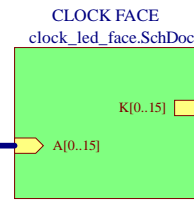
Ambient Light Sensor



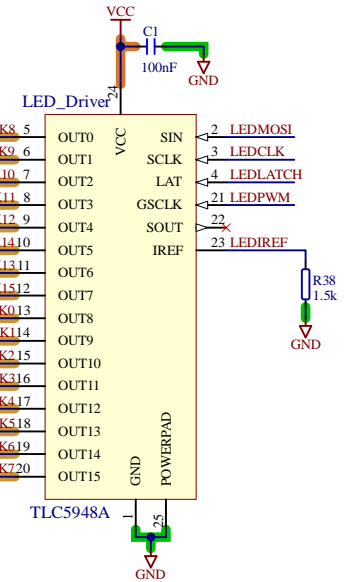
Anode switches

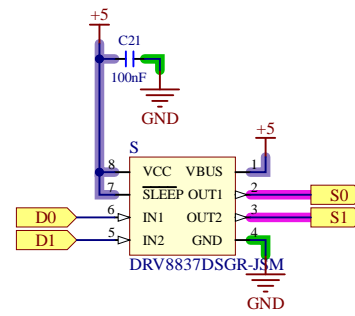


LEDs



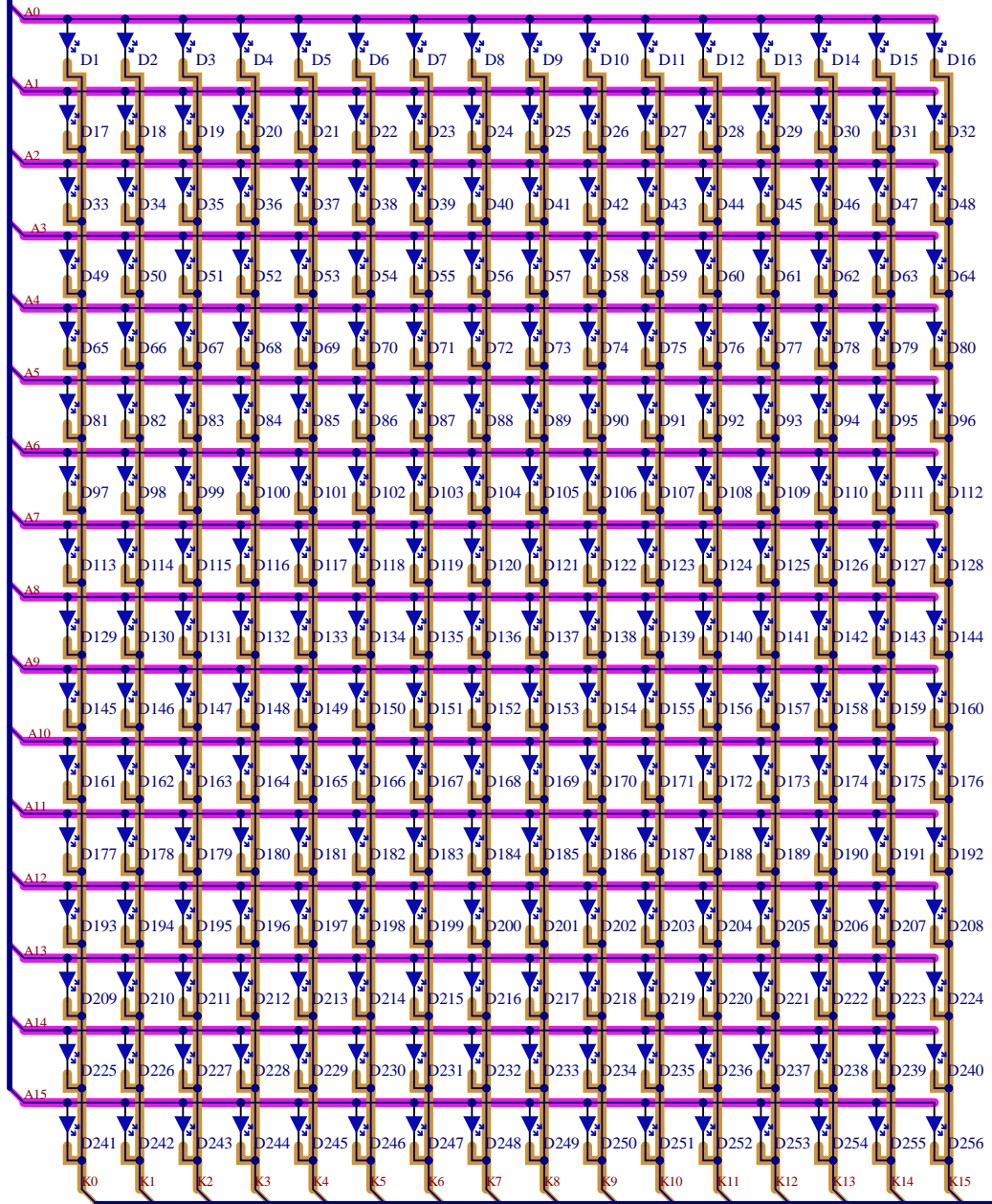
LED Driver





Dual anode switch	Saved on 08 Feb 2026
chs	Sheet 2 of 3

A[0..15]



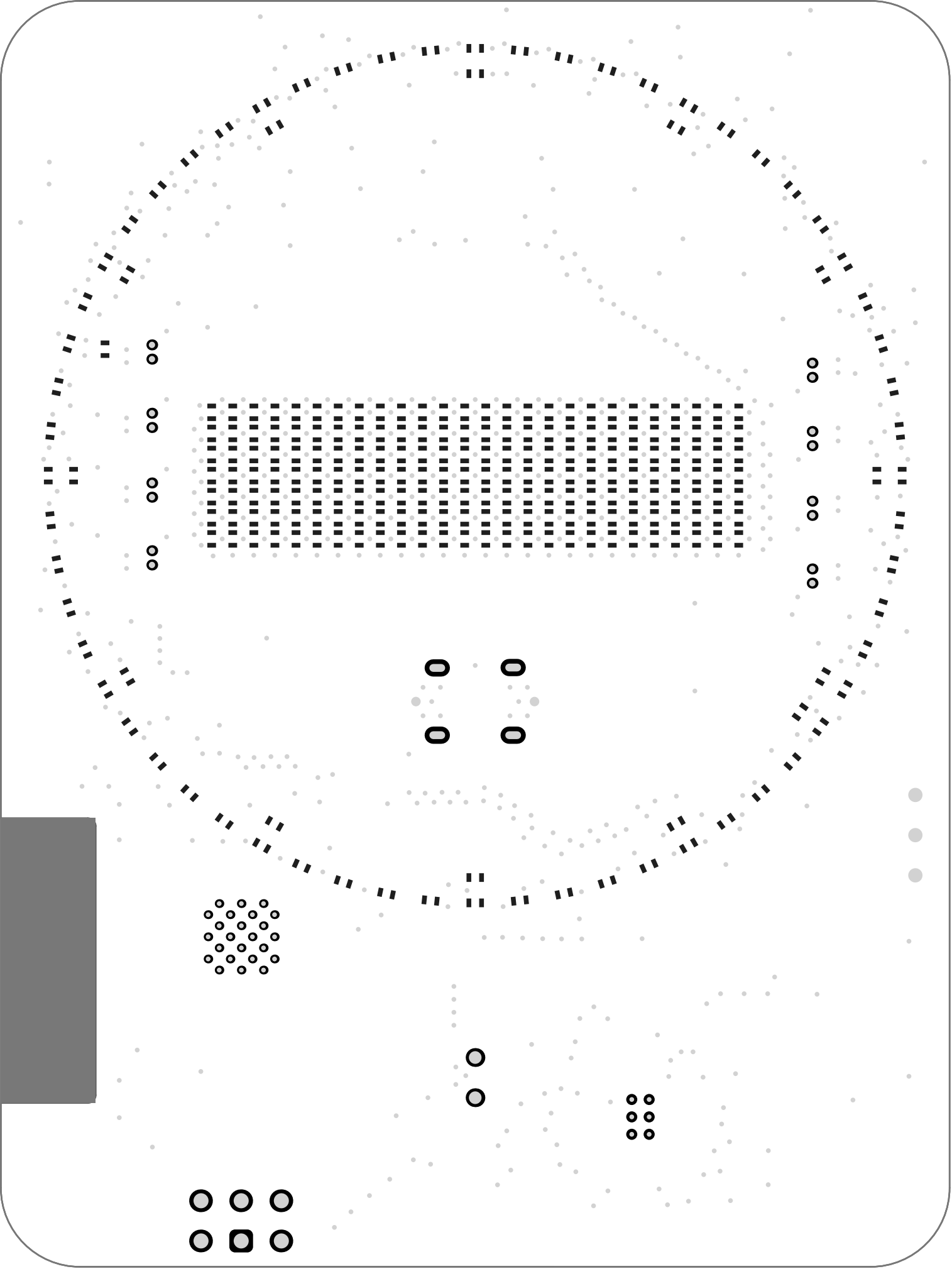
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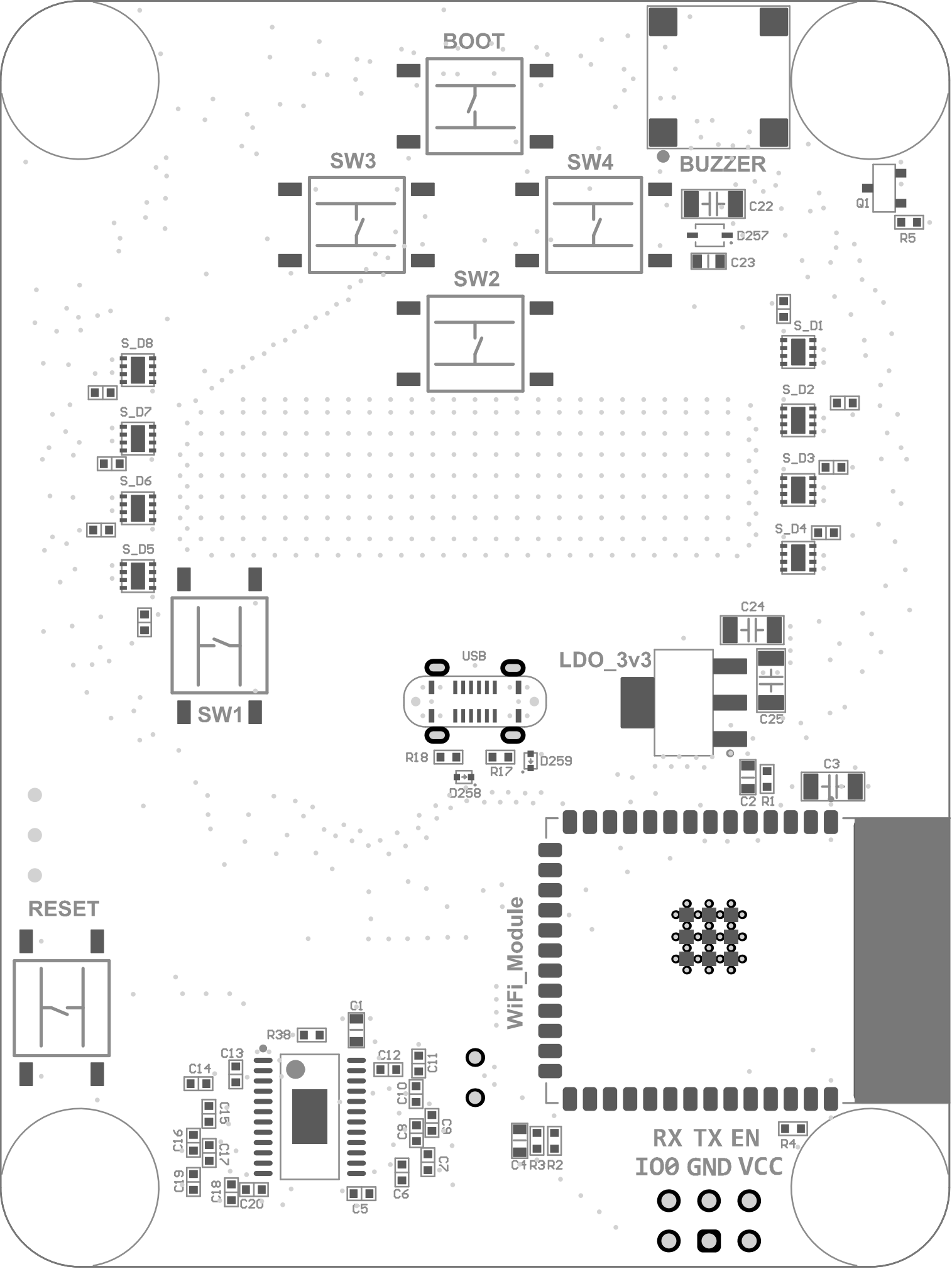
Display

Saved on 19 Dec 2025

chs

Sheet 3 of 3





BOOT

SW3

SW4

BUZZER

SW2

S_D8

S_D7

S_D6

S_D5

S_D1

S_D2

S_D3

S_D4

SW1

USB

LDO_3v3

C24

R18

D258

R17

D259

C25

C2

R1

C3

RESET

WiFi_Module

C14

C13

R38

C1

C12

C11

C10

C9

C8

C7

C6

C5

C16

C15

C17

815

C20

C5

C6

C7

C2

C4

R3

RX TX EN
I00 GND VCC

R4

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for clock_led.PriJPct

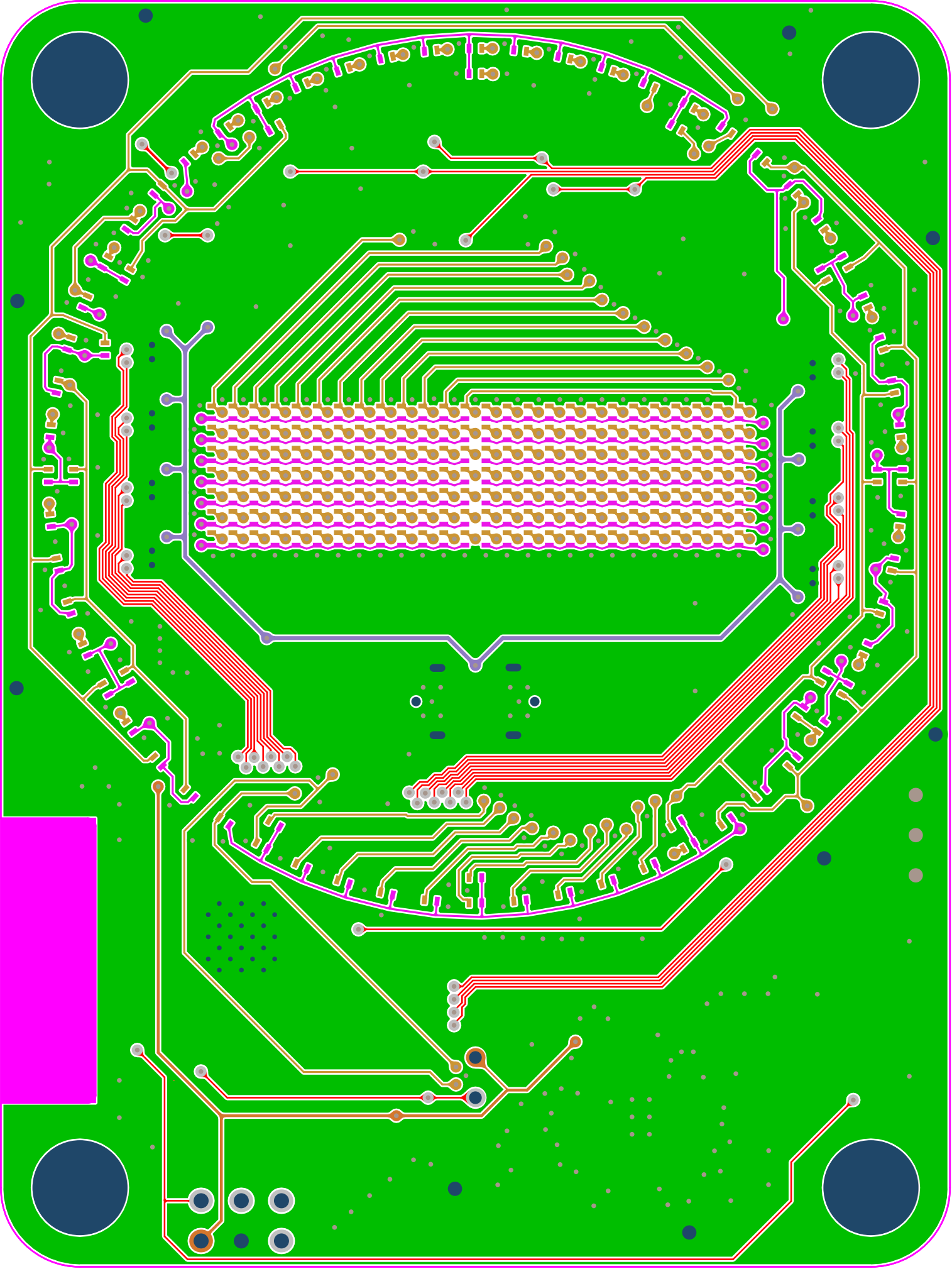
Design Rules Verification Report

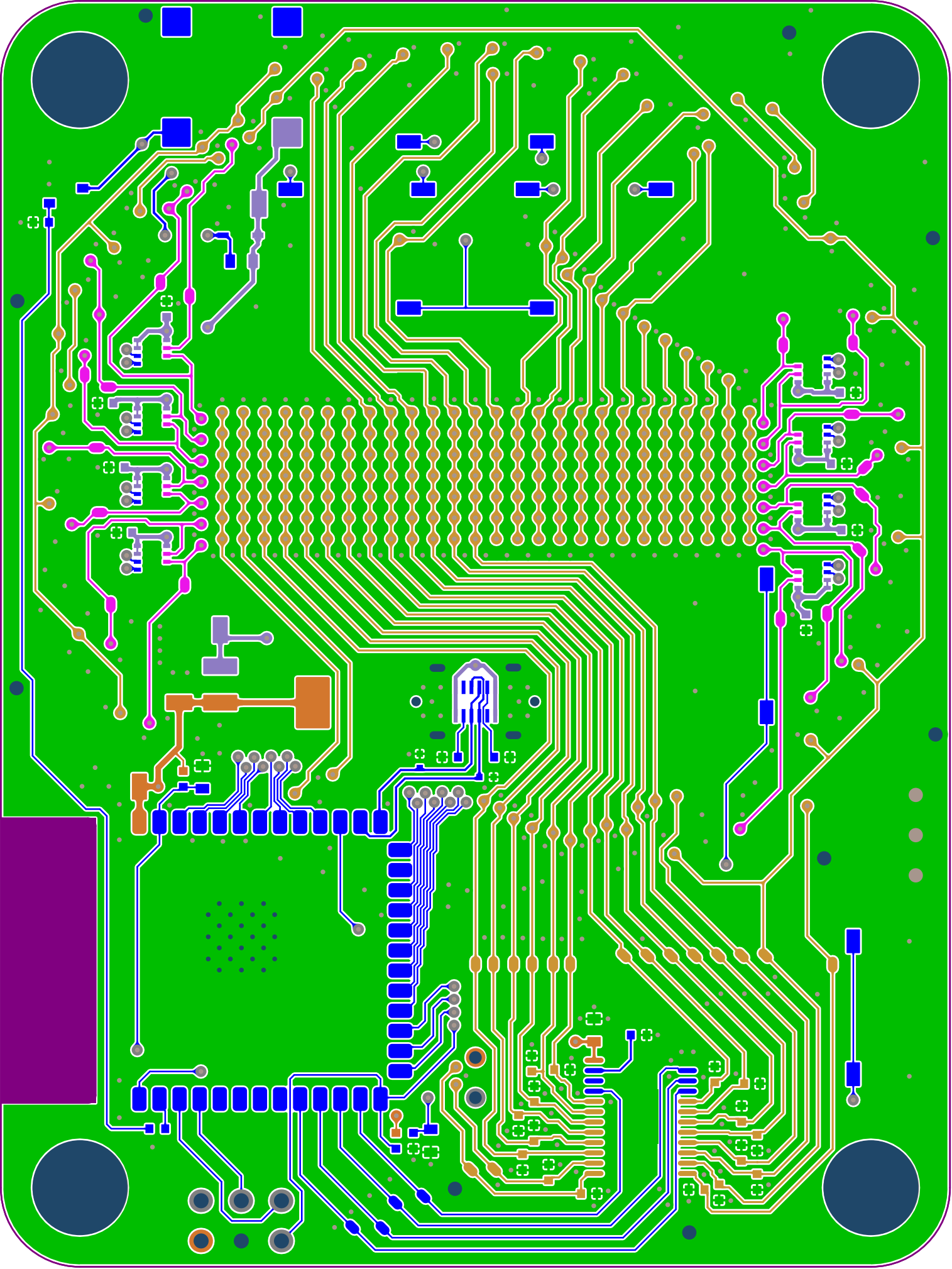
Filename : E:\dev\clock_monsieur\pcb\clock_led.PcbDoc

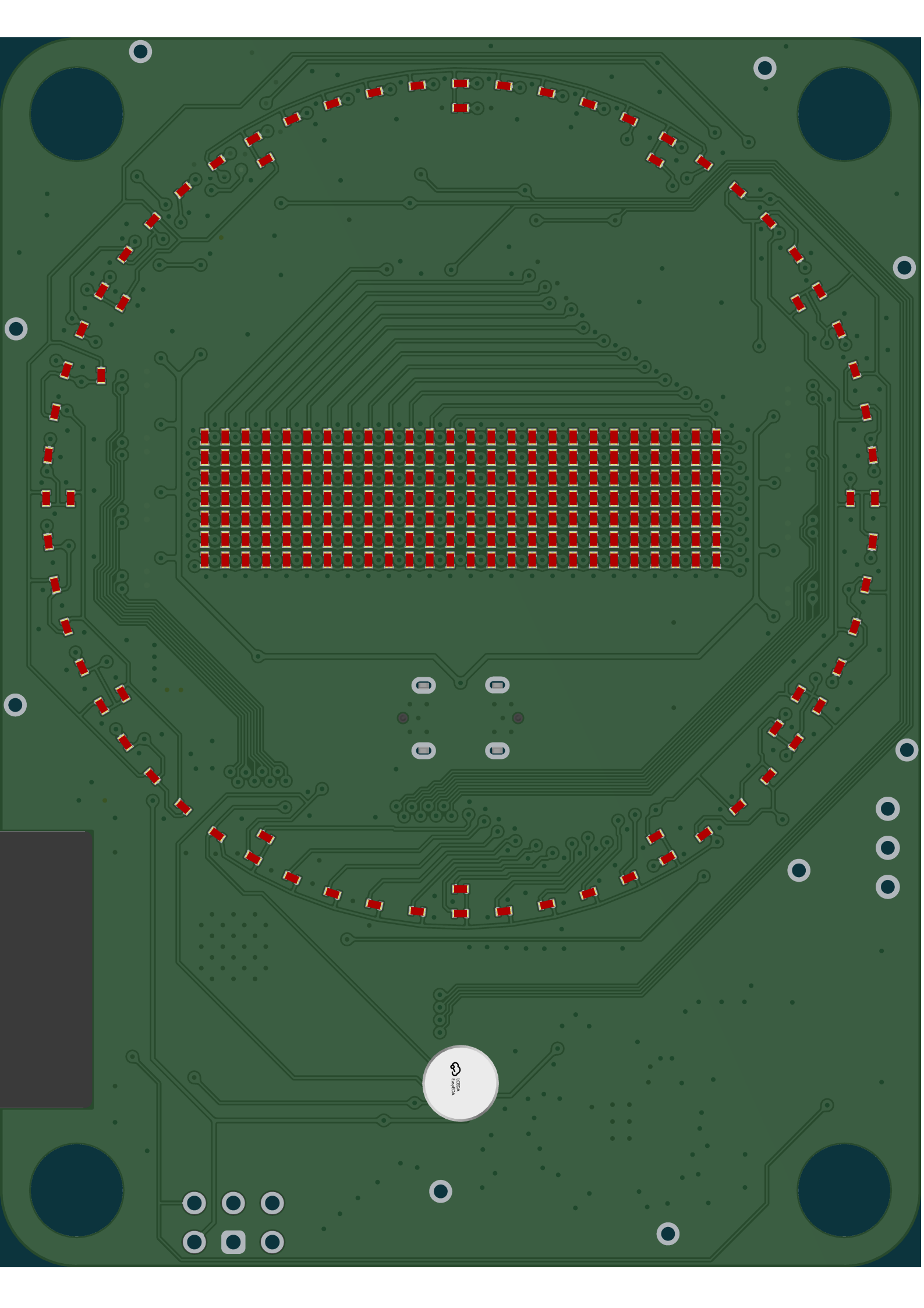
Warnings 0
Rule Violations 0

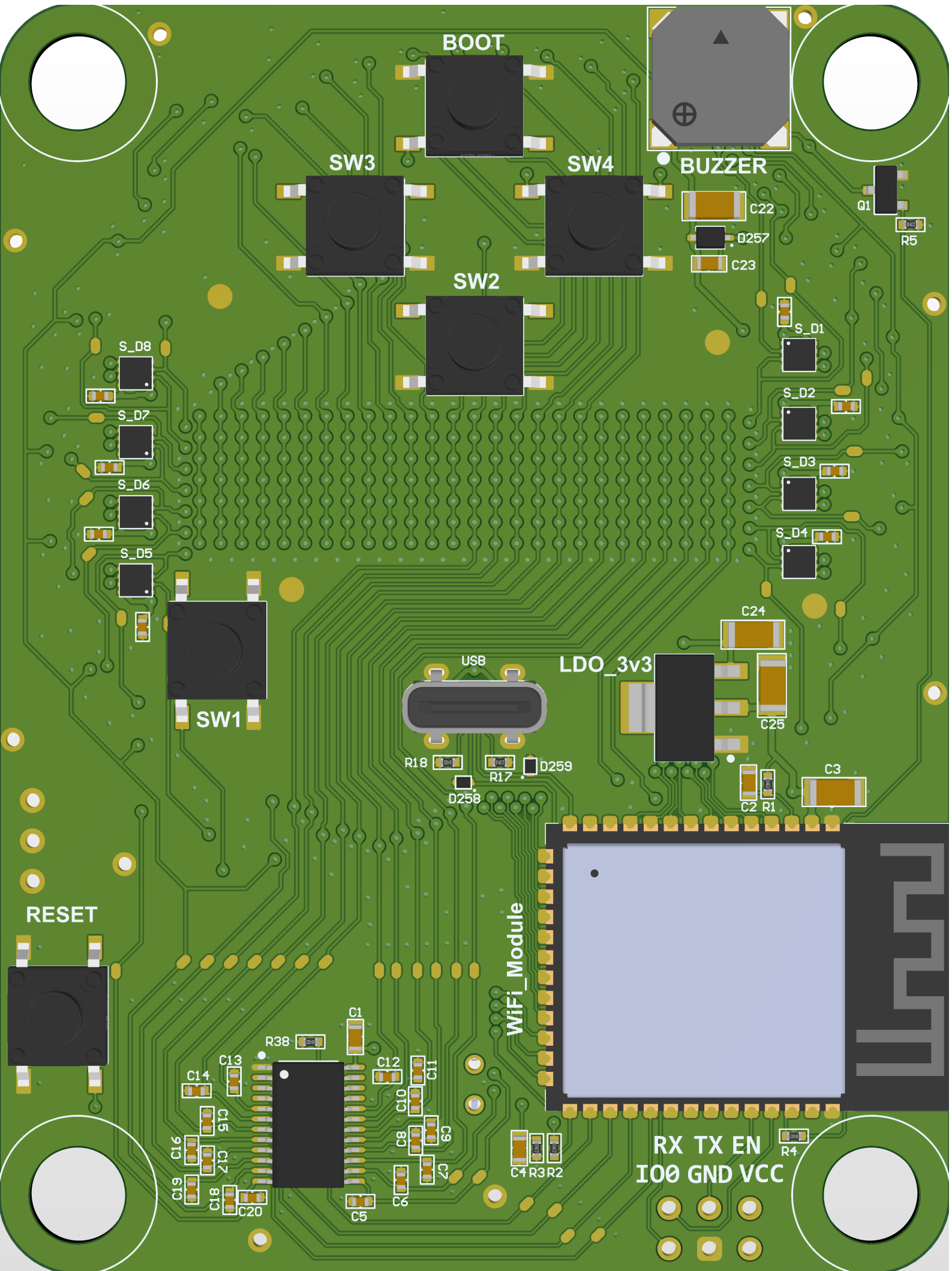
Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.102mm) (All),(All)	0
Clearance Constraint (Gap=0.102mm) (InNetClass('CATHODES')),(InNetClass('CATHODES'))	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint (All)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.076mm) (Max=1mm) (Preferred=0.102mm) (All)	0
Routing Layers(All)	0
Routing Via (Templates Used To Check Via: GND_VIA, LED_ROUTING, SW_ROUTING, S_ROUTING)	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.254mm) (Max=0.254mm) (Preferred=0.254mm)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=6mm) (All)	0
Pads and Vias to follow the Drill pairs settings	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.1mm) (All),(All)	0
Silk To Solder Mask (Clearance=0mm) (False),(All)	0
Silk to Silk (Clearance=0mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Component Clearance Constraint (Horizontal Gap = 0.125mm, Vertical Gap = 0.254mm) (All),(All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	0









BOOT

SW3

SW4

BUZZER

SW2

C22

D257

C23

Q1

R5

S_D1

S_D2

S_D3

S_D4

S_D8

S_D7

S_D6

S_D5

SW1

USB

LDO_3v3

C24

C25

R18

R17

D259

D258

C2

R1

C3

RESET

WiFi_Module

R38

C1

C12

C11

C10

C9

C8

C7

C6

C5

C4 R3 R2

RX TX EN
IO0 GND VCC

R4

C14

C13

C16

C15

C19

C18

C20